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10/697,773	10/29/2003	Hung-Yi Kuo	JCLA10908	8873

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EXAMINER	
STIGLIC, RYAN M	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,773	KUO, HUNG-YI	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8 and 10-18* is/are rejected.

7)☒ Claim(s) *3 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are pending and have been examined.

2. Claims 1-2, 4-8 and 10-18 are rejected.

3. Claims 3 and 9 are objected to.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 recites the limitation "the inhibiting signal" in line 17 of page 11. There is insufficient antecedent basis for this limitation in the claim. The purpose of the inhibiting signal is unclear from the recited claim limitations.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 5-6, 8, 11-12 and 14-17 rejected under 35 U.S.C. 103(a) as being unpatentable over The PCI to PCI Bridge Architecture Specification revision 1.1 in view of Okazawa et al. (US 5,668,956)).

The PCI to PCI Bridge Architecture Specification (hereinafter PCI Bridge) discloses a bridge (Fig. 1-2, page 13) that connects two PCI buses. A set of configuration registers within the bridge contains information relevant to the functionality of the bridge. In order for a processor of the computer system to have access to the configuration registers a configuration transaction (cycle) must be initiated on the primary bus (where the primary bus is the upstream bus). The configuration transaction is summarized by two types of transactions, a type 0 configuration transaction and a type 1 configuration transaction. Type 1 configuration transactions are configuration cycles that are destined for a device/bridge not residing on the primary bus. In other words, if a type 1 configuration command is received by the bridge the type 1 configuration command will be forwarded to a subordinate bus for further processing. In contrast, a type 0 configuration transaction is a configuration cycle that is destined for devices/bridges on the primary bus. "A Type 0 configuration transaction is not forwarded across a bridge but is used to configure a bridge...(page 19)" Therefore the PCI to PCI Bridge Architecture Specification teaches that Type 0 configuration cycles are *inhibited* from re-transmission. While some inherent bus cycle inhibiting circuit and bus bridging circuit means are present, the PCI to PCI Bridge Architecture Specification does not expressly teach the structure of such circuits.

Okazawa teaches a bus bridge (Fig. 1 & 4, 103) used to connect a primary bus (Fig. 1 & 4, 111) and secondary bus (Fig. 1 & 4, 113). Okazawa teaches inhibiting re-transmission of bus cycles onto a secondary bus when the destination of the bus cycle is not the secondary bus. Instead of

re-transmitting the bus cycle to all downstream buses (Fig. 1 & 4, 111, 112, and 113), the bus cycle is only re-transmitted to the proper destination bus (col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) by the connection controller (Fig. 4, 401) and the data path switch (Fig. 4, 402). The connection controller **401** receives bus cycles from the connected buses and decodes bus cycles to output an indicator signal (code information outputted from the sequencer 613 of Fig. 6). The indicator signal is further decoded into a plurality of inhibiting signals (Fig. 5, 511-513; and Fig. 6, 618-621) that inhibit the re-transmission of bus cycles on a subordinate bus.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the bus cycle inhibiting and bus bridging circuit of Okazawa into a bridge compliant with the PCI to PCI Bridge Architecture Specification such that maximization of the utilization efficiency of buses connected to the control chip/bridge is achieved (Okazawa, col. 11, line 64- col. 12, line 4).

For claims 1 and 14 PCI Bridge in view of Okazawa teaches:

A control chip with a bus cycle inhibiting function for preventing internal bus cycle type of the control chip, picked up from a first bus, from being re-transmitting to a second bus of the control chip (PCI to PCI Bridge Architecture Specification, page 13), the control chip comprising:

- a bus cycle inhibiting circuit (Okazawa; Fig. 6, 613) for receiving a bus cycle from the first bus and outputting an inhibiting signal once the bus cycle is determined to be an internal bus cycle type of the control chip (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16); and

- a bus bridging circuit coupled to the bus cycle inhibiting circuit for inhibiting the re-transmission of the bus cycle on receiving the inhibiting signal (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16).

For claims 2 and 16 PCI Bridge in view of Okazawa teaches:

The control chip of claim 1, wherein the bus cycle inhibiting circuit comprises:

- a bus resource decode circuit for receiving a bus cycle from the first bus and outputting an indicator signal representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle type of the control chip (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16; Fig. 6, 609-610); and
- a logic circuit for outputting the inhibiting signal according to a preset enable value (Okazawa; Fig. 6, 607-608 are registers/latches that store control signals from each of the processor and system buses (col. 8, ll. 19-34). Here the control signals represent the present/state of the respective bus, therefore the control signals stored in the latches act as enable signals) and the indicator signal (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16; Fig. 6, 614; Fig. 5, 510).

For claims 5 and 11 PCI Bridge in view of Okazawa teaches:

The control chip of claim 2, wherein the preset enable value is stored inside a register (Okazawa; col. 8, ll. 19-34; Fig. 6, 607-608).

For claims 6, 12 and 17 PCI Bridge in view of Okazawa teaches:

The control chip of claim 1, wherein the second bus comprises a peripheral component interconnect (PCI) bus (PCI Bridge; page 12).

For claim 8 PCI Bridge in view of Okazawa teaches:

A bus cycle inhibiting circuit for a control chip having at least a first bus and a second bus, comprising:

- a bus resource decode circuit for receiving a bus cycle from the first bus (Okazawa; Fig. 6, 613; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) and outputting an indicator signal (Fig. 6, Code Information from 613) representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle; and
- a logic circuit (Okazawa; Fig. 6, 614; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16) for outputting the inhibiting signal (Okazawa; Fig. 6, 618-621) according to a preset enable value (Okazawa; Fig. 6, 607-608 are registers/latches that store control signals from each of the processor and system buses (col. 8, ll. 19-34). Here the control signals represent the present/state of the respective bus, therefore the control signals stored in the latches act as enable signals) and the indicator signal (Okazawa; col. 7, ll. 10-49; col. 8, line 12 – col. 9, line 16).

For claim 15 PCI Bridge in view of Okazawa teaches:

The bus cycle inhibiting method of claim 14, wherein the inhibiting signal is issued when the bus cycle is found to be an internal input/output bus cycle, an internal memory bus cycle or an internal configuration bus cycle (PCI Bridge; page 19).

8. Claims 7, 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over PCI to PCI Bridge Architecture Specification in view Okazawa as applied to claims 1, 8 and 14 above, and further in view of what was well known at the time of Applicant's invention as evidenced by Gulick (US 5,926,629).

As previously discussed PCI Bridge in view of Okazawa teach a bridge that inhibits the re-transmission of internal bus cycles received from a primary bus. The PCI Bridge comprises a bus cycle inhibiting circuit for detecting the presence of an internal bus cycle and a bus bridging circuit for inhibiting the re-transmission of the internal bus cycle on a secondary bus. Neither PCI Bridge nor Okazawa however explicitly teach of the bridge being a well known Southbridge.

Gulick teaches a Southbridge (Fig. 2 & 3, 201) that connects to a Northbridge of the computer system through a primary bus. The Southbridge provides a connection between the system processor(s), via the Northbridge, and a plurality of peripheral buses (i.e. Fig. 3, USB Controller, EIDE Controller, ISA Bus 307). Therefore the Southbridge is solely responsible for increasing

the performance of the system by providing interfaces to a plurality of I/O devices and various other peripherals (col. 4, line 63 – col. 6, line 25).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement a Southbridge as the bridge of PCI Bridge in view of Okazawa such that the system of PCI Bridge in view of Okazawa is provided with the expansion capabilities of a Southbridge.

9. Claims 1-2, 4-8 and 10-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US005935226A) in view of PCI to PCI Bridge Architecture Specification.

Klein discloses a PCI compliant Southbridge (Fig. 2 & 3, 70) installed in a computer system (Fig. 1, 50). The PCI compliant Southbridge discloses a system and method of inhibiting re-transmission of bus cycles from the PCI bus (Fig. 2 & 3, 66) and destined for the ISA bus (Fig. 2 & 3, 72). The Southbridge device contains a bus cycle inhibiting circuit (Fig. 3, 112) for receiving a bus cycle from the PCI/first bus and outputting an inhibiting signal (Fig. 3, Output from OR gate 120) once the bus cycle is determined to be a bus cycle for a particular I/O device (col. 5, line 23 – col. 7, 12). The Southbridge further comprises a bus bridging circuit (Fig. 3, items 100,108) for inhibiting the re-transmission of the bus cycle to the particular I/O device (col. 7, ll. 4-12). While the PCI compliant Southbridge discloses a detailed explanation of the bus cycle inhibiting circuit and bus bridging circuit, the PCI compliant Southbridge does not show all components required of PCI compliant bridging devices as noted by PCI Bridge.

The PCI to PCI Bridge Architecture Specification (hereinafter PCI Bridge) discloses a bridge (Fig. 1-2, page 13) that connects two PCI buses. A set of mandatory configuration registers (Fig. 1-2, page 13) within the bridge contains information relevant to the functionality of the bridge. In order for a processor of the computer system to have access to the configuration registers a configuration transaction (cycle) must be initiated on the primary bus (where the primary bus is the upstream bus). The configuration transaction is summarized by two types of transactions, a type 0 configuration transaction and a type 1 configuration transaction. Type 1 configuration transactions are configuration cycles that are destined for a device/bridge not residing on the primary bus. In other words, if a type 1 configuration command is received by the bridge the type 1 configuration command will be forwarded to a subordinate bus for further processing. In contrast, a type 0 configuration transaction is a configuration cycle that is destined for devices/bridges on the primary bus. "A Type 0 configuration transaction is not forwarded across a bridge but is used to configure a bridge...(page 19)" Therefore the PCI to PCI Bridge Architecture Specification teaches that Type 0 configuration cycles are *inhibited* from re-transmission. While some inherent bus cycle inhibiting circuit and bus bridging circuit means are present, the PCI to PCI Bridge Architecture Specification does not expressly teach the structure of such circuits. By implementing the bus cycle inhibiting circuit (Fig. 3, 112) and bus bridging circuit (Fig. 3, 100, 108) of Klein the PCI compliant Southbridge is able to inhibit the re-transmission of Type 0 configuration transactions as required by the PCI Bridge Specification.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the bus cycle inhibiting and bus bridging circuits of Klein to perform the required Type 0 configuration downstream re-transmission inhibiting of the PCI Bridge Specification in order for the Southbridge to be truly PCI compliant.

For claims 1 and 14 Klein in view of PCI Bridge teaches:

A control chip (Klein; Fig. 2 & 3, 70) with a bus cycle inhibiting function for preventing internal bus cycle type of the control chip, picked up from a first bus, from being re-transmitting to a second bus of the control chip, the control chip comprising:

- a bus cycle inhibiting circuit (Fig. 3, 112) for receiving a bus cycle from the first bus and outputting an inhibiting signal (Klein; output of OR gate 120 of Fig. 3) once the bus cycle is determined to be an internal bus cycle type of the control chip (Klein; col. 5, line 23 – col. 7, 12); and
- a bus bridging circuit coupled to the bus cycle inhibiting circuit for inhibiting the re-transmission of the bus cycle on receiving the inhibiting signal (Klein; col. 7, ll. 4-12).

For claims 2, 8 and 16 PCI Bridge in view of Okazawa teaches:

The control chip of claim 1, wherein the bus cycle inhibiting circuit comprises:

- a bus resource decode circuit (Fig. 3, 112) for receiving a bus cycle from the first bus and outputting an indicator signal (Fig. 3, outputs of bus resource decode circuit 112) representing the particular type of bus cycle when the bus cycle is determined to be an

internal bus cycle (PCI BRIDGE; type 0 configuration, page 19) type of the control chip (Klein; Fig. 3, 112; Klein; col. 5, line 23 – col. 7, 12); and

- a logic circuit for outputting the inhibiting signal (Fig. 3, output of OR gate 120) according to a preset enable value (Klein; Fig. 3, items 116-120; col. 5, line 23 – col. 7, 12) and the indicator signal (Klein; col. 5, line 23 – col. 7, 12).

For claims 4 and 10 Klein in view of PCI Bridge teaches:

The control chip of claim 2, wherein the logic circuit comprises AND gates and OR gates (Klein; Fig. 3, items 116-120).

For claims 5 and 11 Klein in view of PCI Bridge teaches:

The control chip of claim 2, wherein the preset enable value is stored inside a register (Klein; col. 5, line 23 – col. 7, 12; Fig. 3 items 114 and 124).

For claims 6, 12 and 17 Klein in view of PCI Bridge teaches:

The control chip of claim 1, wherein the second bus comprises a peripheral component interconnect (PCI) bus (Klein; col. 4, ll. 34-38; PCI Bridge, page 12).

For claims 7, 13 and 18 Klein in view of PCI Bridge teaches:

The bus cycle inhibiting circuit of claim 8, wherein the control chip comprises a South-bridge control chip (Klein; Fig. 2 & 3. 70).

For claim 15 Klein in view of PCI Bridge teaches:

The bus cycle inhibiting method of claim 14, wherein the inhibiting signal is issued when the bus cycle is found to be an internal input/output bus cycle, an internal memory bus cycle or an internal configuration bus cycle (PCI Bridge; page 19).

Allowable Subject Matter

10. Claims 3 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Kao discloses a Southbridge device configurable through internal bus configuration cycles.

b. Joshi disclose a Southbridge device that maintains an internal event log.

c. Porterfield discloses various bus bridges with shadowed configuration registers that are accessible through internal configuration bus cycles.

d. Creta discloses a mechanism for converting internal configuration bus cycles into I/O transactions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAUL R. MYERS
PRIMARY EXAMINER

RMS